The MET-1

MAGNETIC TAPE AND PAPER CHART READER

Schematics and Circuit Description

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Magnetic Tape and Paper Chart Reader

This unit serves two functions: it reads NRZ encoded magnetic tape, and reads a pointer position for use with a paper chart reader. The unit serves as an interface between the tape deck and chart reader and a digital computer.

Figure 1 shows the block diagram of the system. The tape deck feeds three data channels and a time channel to the input card. Each of the four channels are treated identically in the input card. The head currents are amplified, fed to comparators, and the original digital signal is then reconstructed. Each of the three data signals is fed to a counter board. The counters count in decimal form the number of pulses on a particular track between time pulses. At the end of each time pulse, the count is stored in latches. This information reaches the computer through the serial interface card. There is a lot of data to be transmitted, so the information is multiplexed onto a single eight bit word for transmission to the computer. The protocol is as follows. Each device has a device number. If the computer wants a particular device's data, it must transmit a command word to the serial interface. The command word specifies the port, or device number for which information is being requested. Immediately after the command word is received, the present contents of the specified device is sent to the computer. Any of the ports may be read in this manner. The chart reader feeds a voltage to the A/D (analog to digital converter) card, which converts the voltage to a binary number between 0 and 255.

In practice, to use the chart reader, the computer transmits a command word to read the status of the A/D converter. The status word of the converter is transmitted to the computer, and the computer reads the information. If the data indicates that the push button is pressed, then the computer will transmit the command word for the A/D data. The serial interface will transmit the A/D data word, and the computer receives it. The computer must then continue transmitting command words to read the status of the A/D card to determine when the push button is released. After this, the process can continue.

A typical process for using the magnetic tape reader

would be as follows. The computer transmits the command word requesting the high word of counter #1 which contains the status of the time pulse. The requested data is sent, and the cycle repeats until the new data available flag is set. At this point, the computer records the counter #1 high word, and then transmits the command word requesting the counter #1 low word. It then receives that data, and records it. In the same manner counters #2 and #3 are read, whereupon the entire cycle repeats. Naturally, the computer may only request some, not all, of the data.

INPUT CARD

Figure 2 shows the schematic of the input card. Each channel drives a differential input amplifier constructed from half of a 558 operational amplifier with a gain of approximately 200. The differential inputs provide a high degree of noise immunity, reduces power line pickup, and improves channel separation. The output of this amplifier is ac coupled to a second amplifier stage with a gain of 5. The quiescent level of this amplifier is Vcc/2, or 2.5 volts. Fire 12 shows the waveforms at various points. The signal at the output of the second amplifier consists of positive and negative pulses, with a zero level of 2.5 volts. This signal drives a pair of comparators. A positive and negative threshold is set about one volt above and below the quiescent point. When the posive pulses exceed the positive threshold, the output of that comparator goes low. Similarly, when the negative pulses exceed in the n9ative direction the negative threshold, the output of the negative comparator goes low. The positive pulses set a flip flop, and the negative pulses reset the flip flop. This results in a reproduction of the original record currents while affording a high degree of noise immunity. This is because more than one positive or negative pulse in a row will have no effect on the output. The ouputs of the flip flops may be seen by the light emitting diodes on the input card. A master reset pulse emanating from the serial interface board upon power up resets all of the flip flops. The necessary timing signals are also generated on the input card. A one shot triggers on the rising edge of the

time pulse, to provide the latch signal. A second one shot triggers on the falling edge of the first one shot, to generate the clear signal for the counters. These signals are shown in fig 13.

COUNTER CARD

The three counter cards are identical, one for each channel. Three decade counters are cascaded to permit counts up to 999. The input comes from the proper channel output on the input card. A flip flop will be set if ohe count exceeds 999, and may either be used to indicate an error condition, or if counts above 999 but less than 1999 are expected, it may be used as a fourth count digit. However, any counts over 1999 will not change the overflow flag. At the acquisition of the time pulse, the counts are latched in the 8212 eight bit latches by the latch pulse from the input card. Immediately thereafter, the clear pulse zeroes the counters and clears the overflow flag. The rising edge of the time pulse also sets a flip flop which may be read as the data available signal. This flip flop is only reset when the output enable lo is placed low. The 8212 latches are tri-state devices, so the data is merely latched internally, and not sent to the serial interface card. If the output enable lo line is placed low which occurs when that port is selected, then the low latch is enabled and it places its data on the data bus. This is then transmitted through the serial interface. When the output enable hi is placed low, the high latch puts its data on the data bus, and the tri-state buffer 74125 puts the data available signal through to the data bus.

A/D CONVERTER CARD

Thvoltage present on the arm of the chart reader goes to the input of the A/D converter chip, a Teledyne 8703. This A/D converter continuously converts the input voltage to a binary number between 0 and 255. The outputs of the A/D converter are tri-state, so the data is not placed on the data bus unls it is requested by the serial interface card. A section of a 74125 is used as a switch debouncer, and feeds a tri-state buffer which enables the push button status to be read in by port #8. At the

same time, the data valid signal and busy signals can be read. The busy signal is of no particlar interest to the user.

SERIAL INTERFACE CARD

The interface card communitates with the computer. The heart of the card is the UART (universal asynchronous receiver transmitter). The UART has two sections: transmit and receive. The receive side operates as follows. The signal from the computer is received and latched in the UART, and appears on pins 5-12. The highest bit drives a transistor which operates the relay which activates the tape reader. The lowest four bits drive a ten bit demultiplexer to provide the port select number. Only one of the ten lines may be low at any time, otherwise several devices would fight for the data bus at the same time and destroy one another. These port select lines go to the counter boards and the A/D card. The transmitter section of the UART sends the data on the input pins 26-33. These pins represent the data bus, and whichever port is selected will provide the data. When the UART receives a character, the output data available pin goes high. This is inverted and sent to the reset data available pin, and also triggers the transmitter data strobe. This last action begins a transmit cycle, and the data on the data bus is sent to the computer. A current loop interface is provided by the inverters and transistors connected to the transmitter serial output and receiver serial input pins of the UART. The UART is strapped for eight data bits and no parity bit.

The UART requires a clock signal 16 times the baud rate desired. A crystal oscillator, 8224, divides the crystal frequency by 9 to give a 2 MHz signal. This drives a divide by 13 counter which feeds four binary dividers. The five baud rates 9600, 4800, 2400, 1200, and 600 may be selected by the DIP switch on the serial interface card. The 8224 also provides upon power up a master reset pulse.

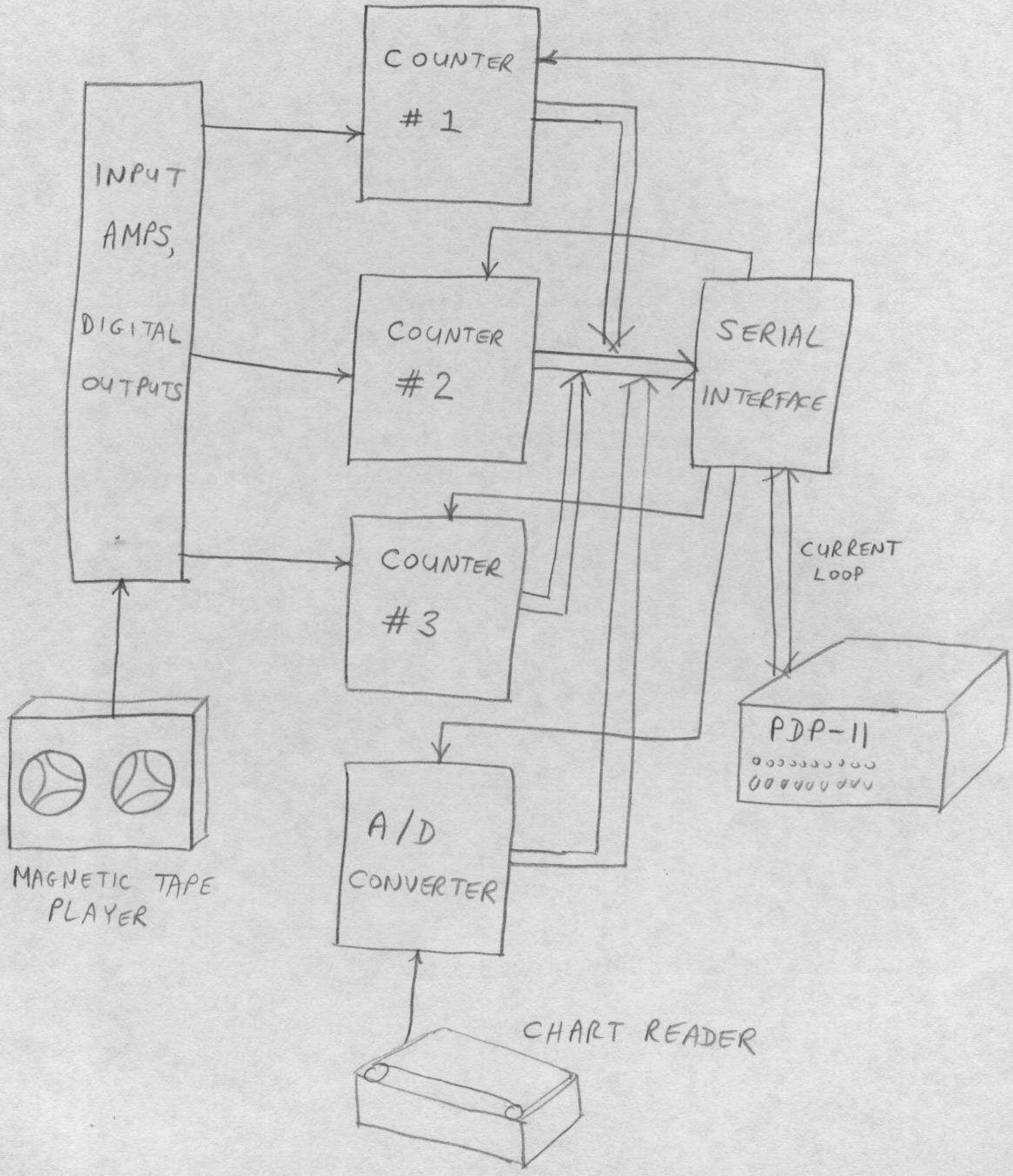


Fig 1 - BLOCK DIAGRAM

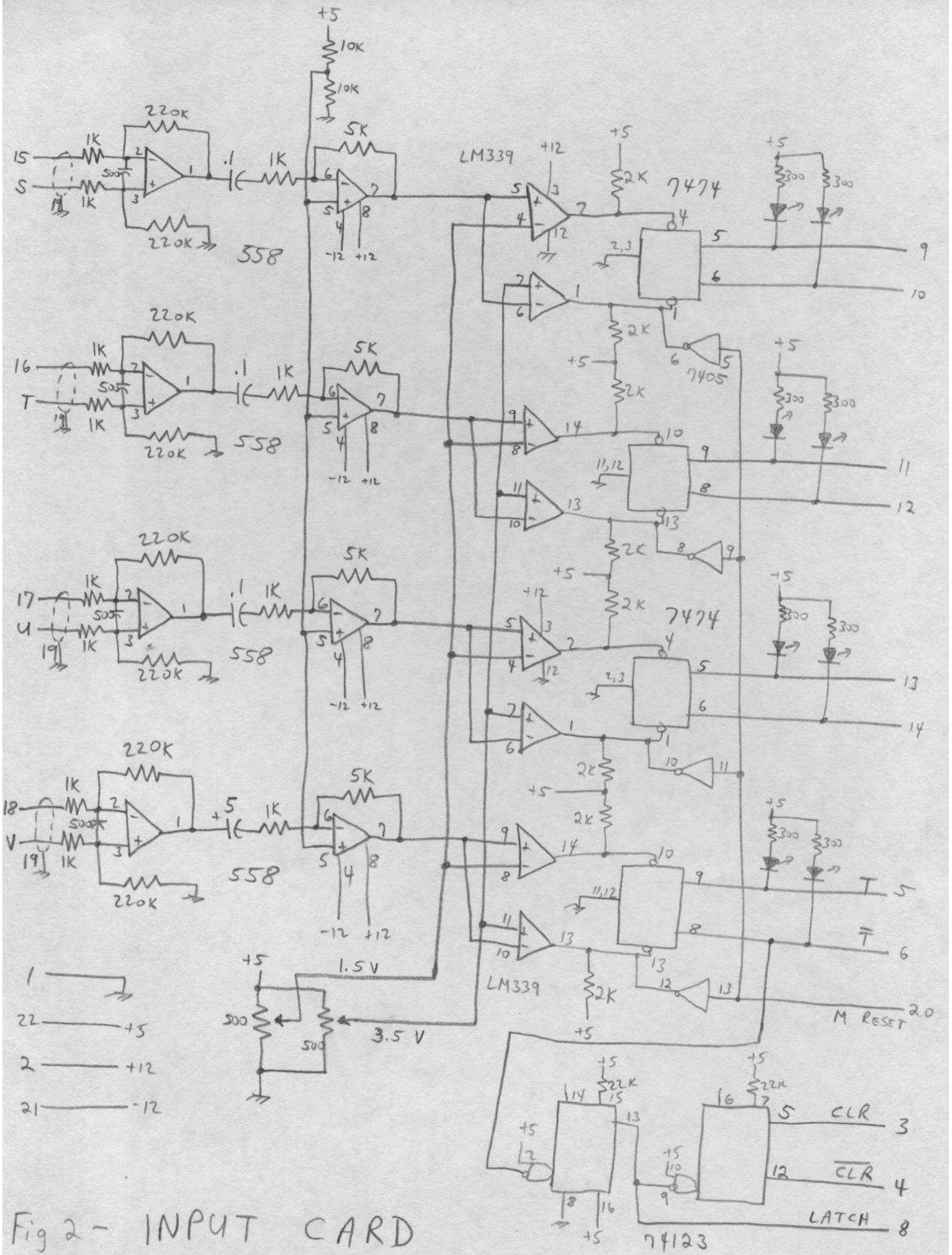


Fig 2- INPUT CARD

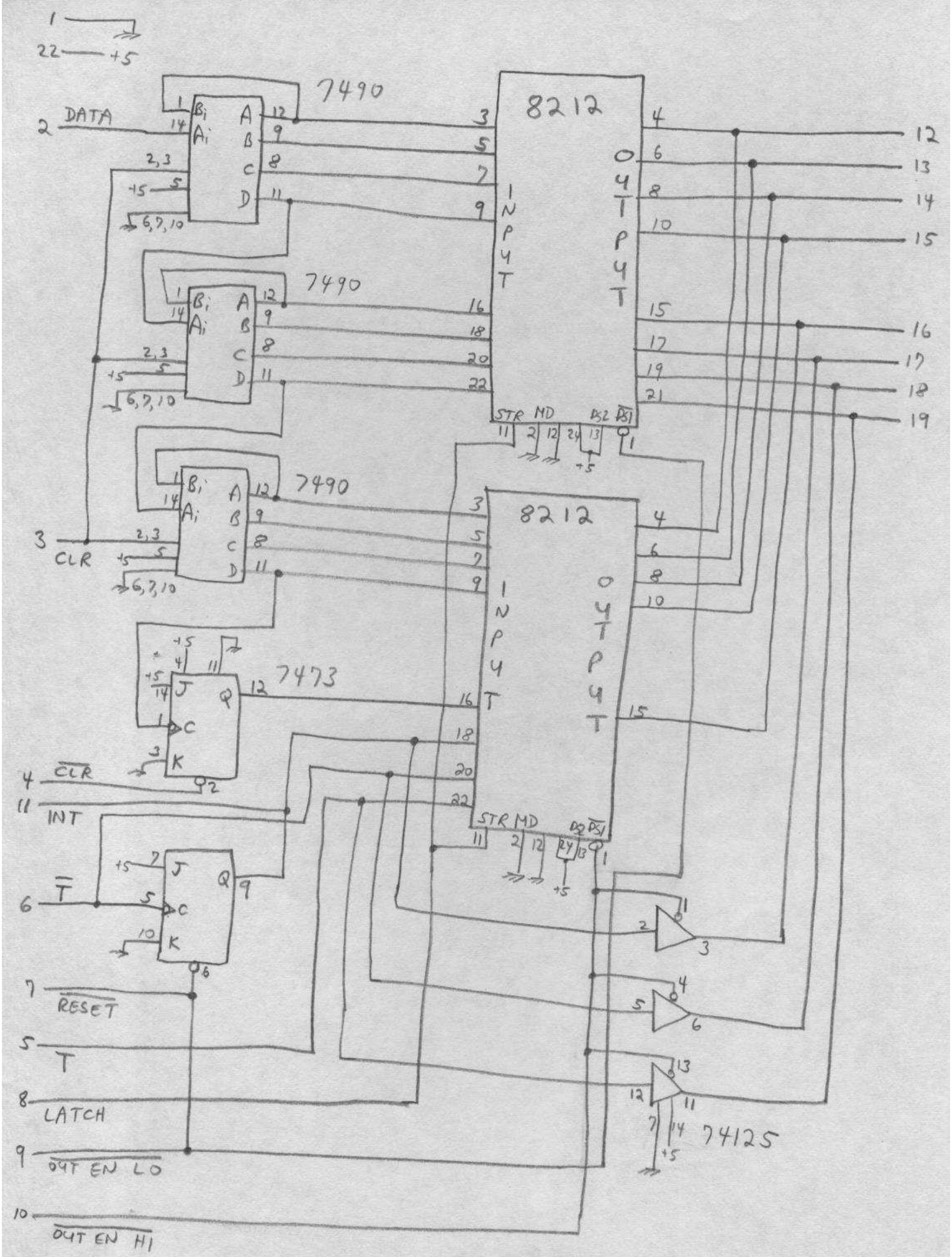


Fig 3 - COUNTER CARD

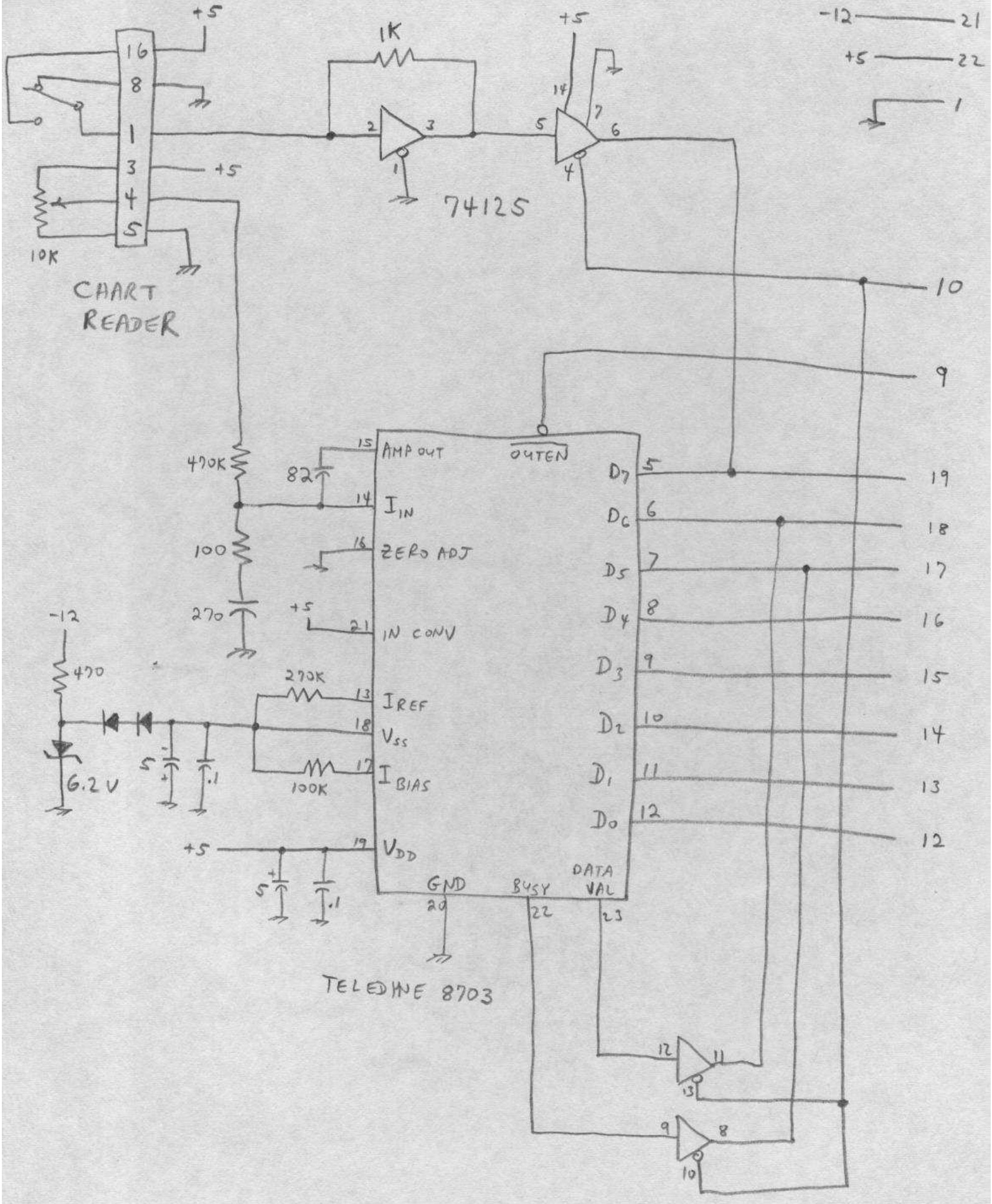


Fig 4 - A/D CONVERTER CARD

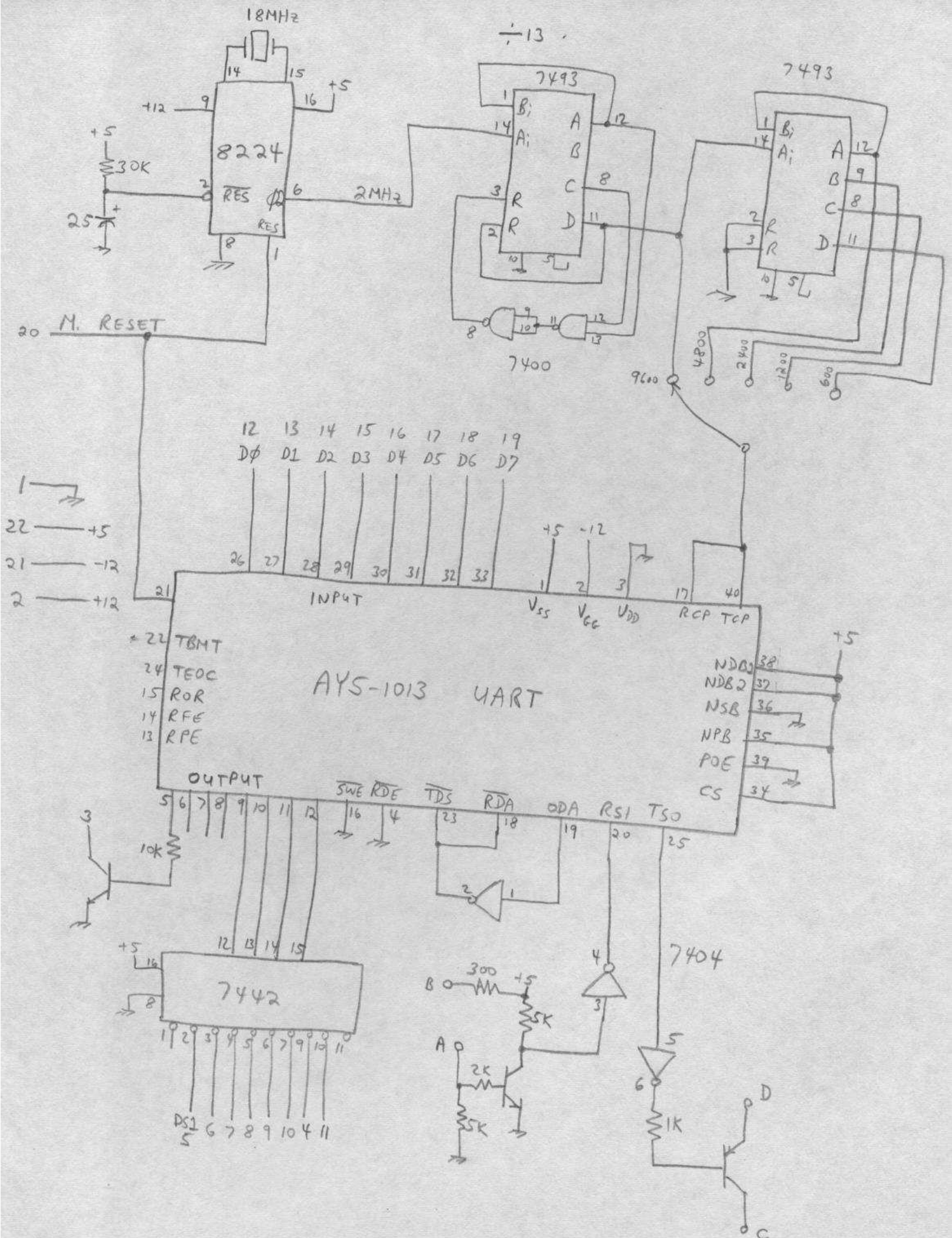


Fig 5- SERIAL INTERFACE CARD

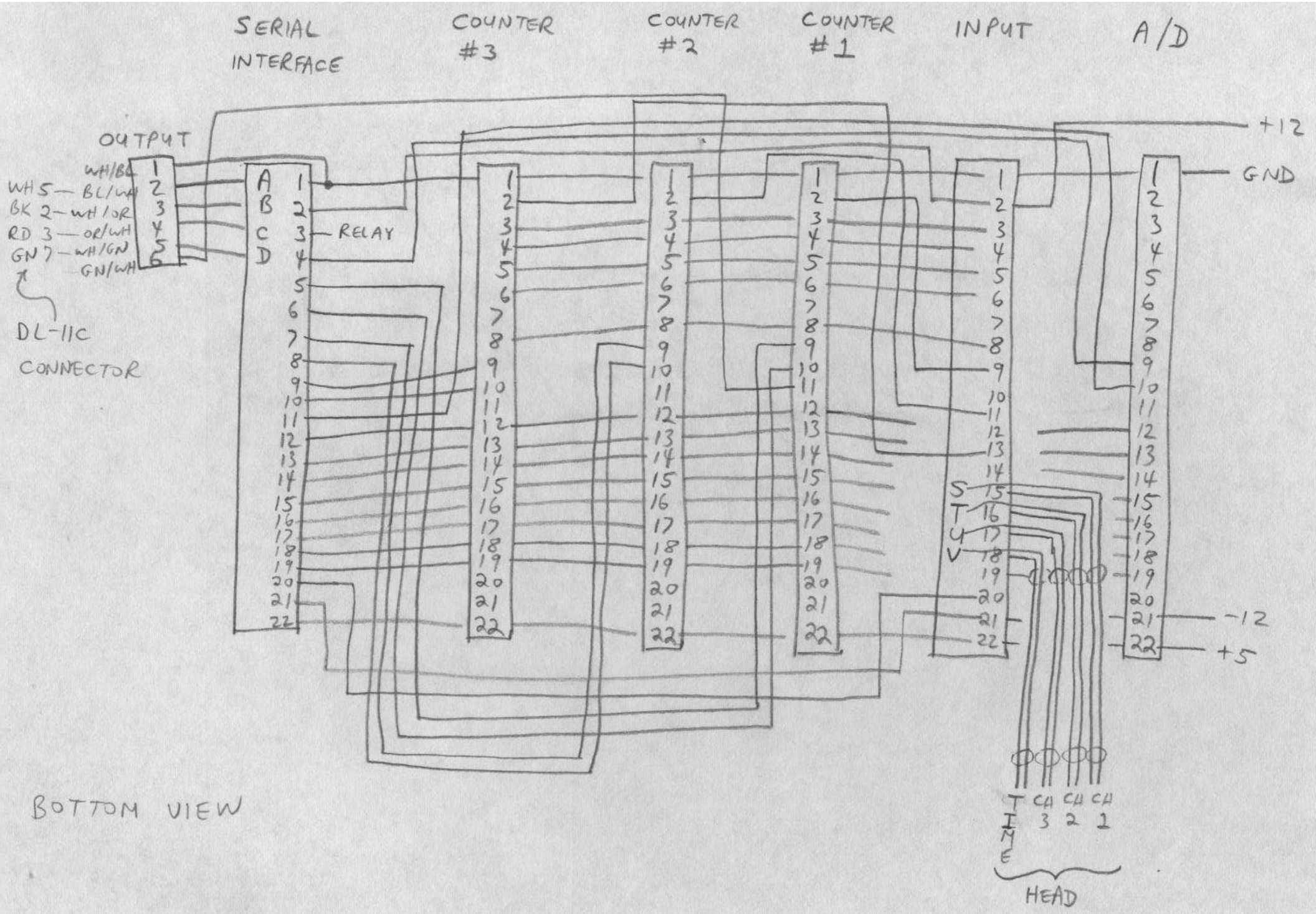


Fig 6 - BACKPLANE WIRING

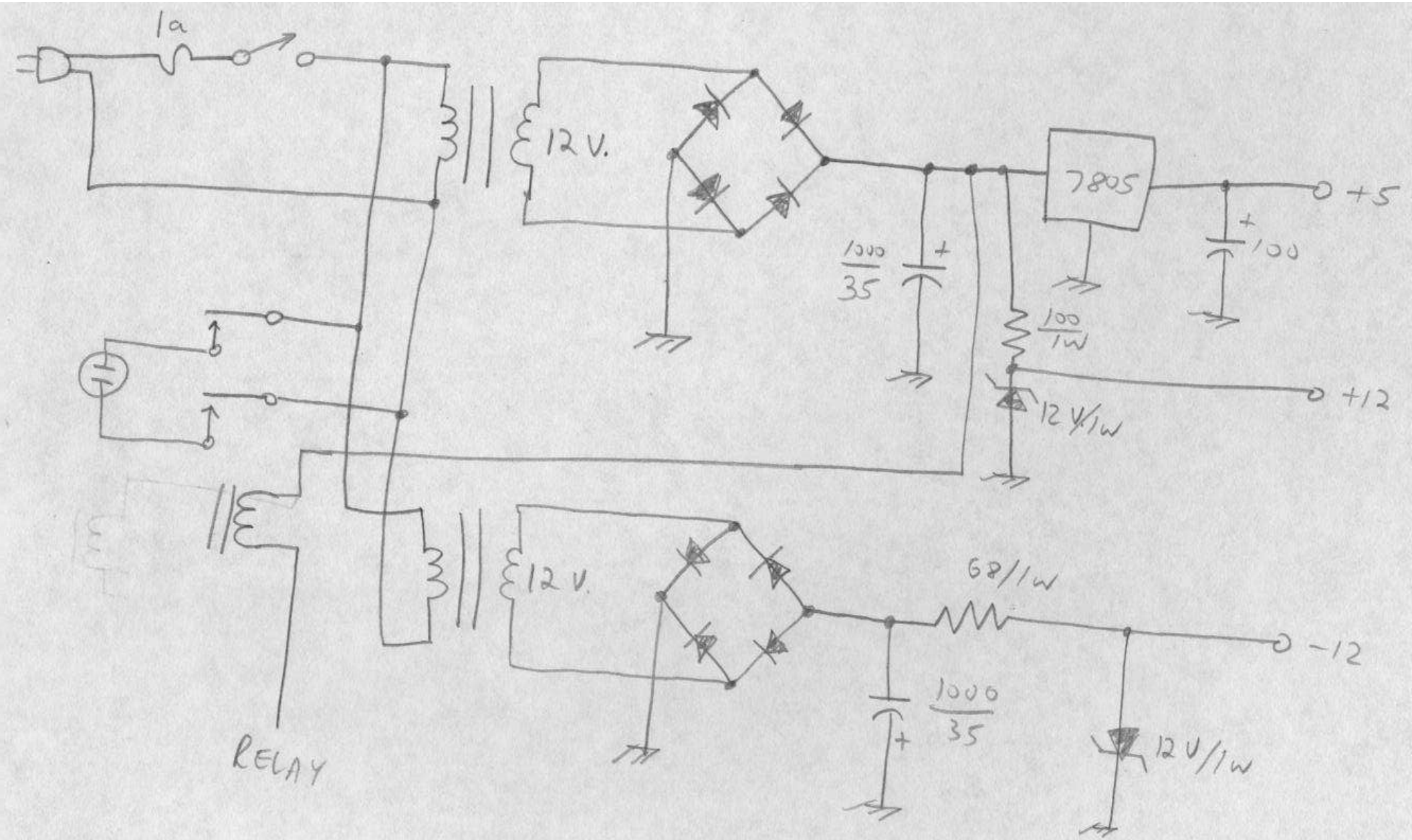
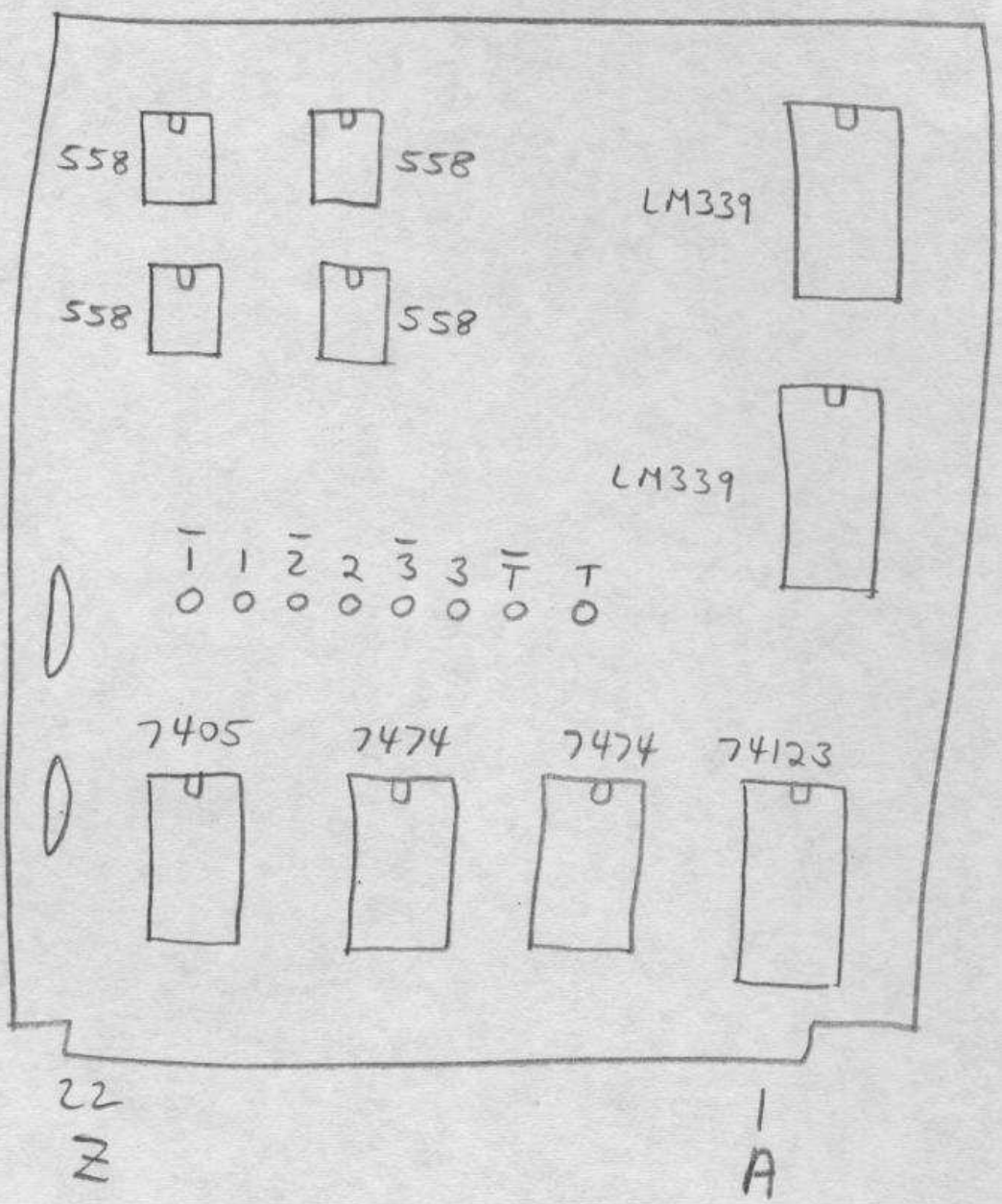


Fig 7 - POWER SUPPLY

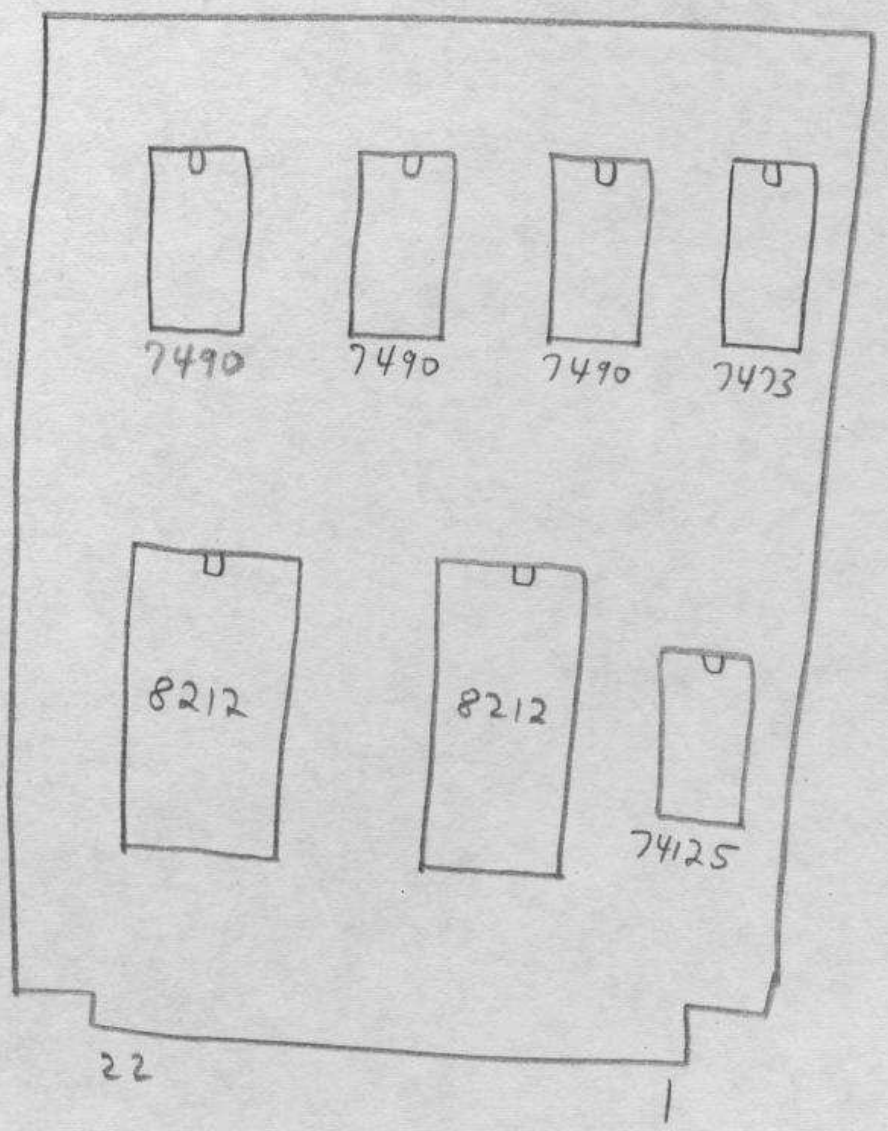
TOP VIEW



INPUT CARD

Fig 8

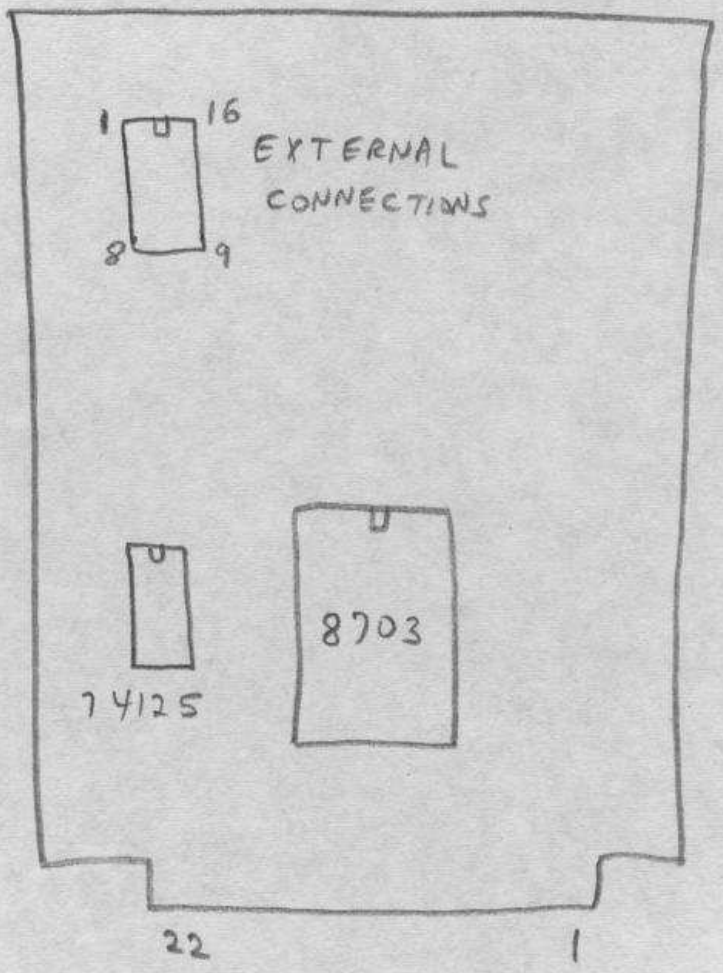
TOP VIEW



COUNTER CARD

Fig 9

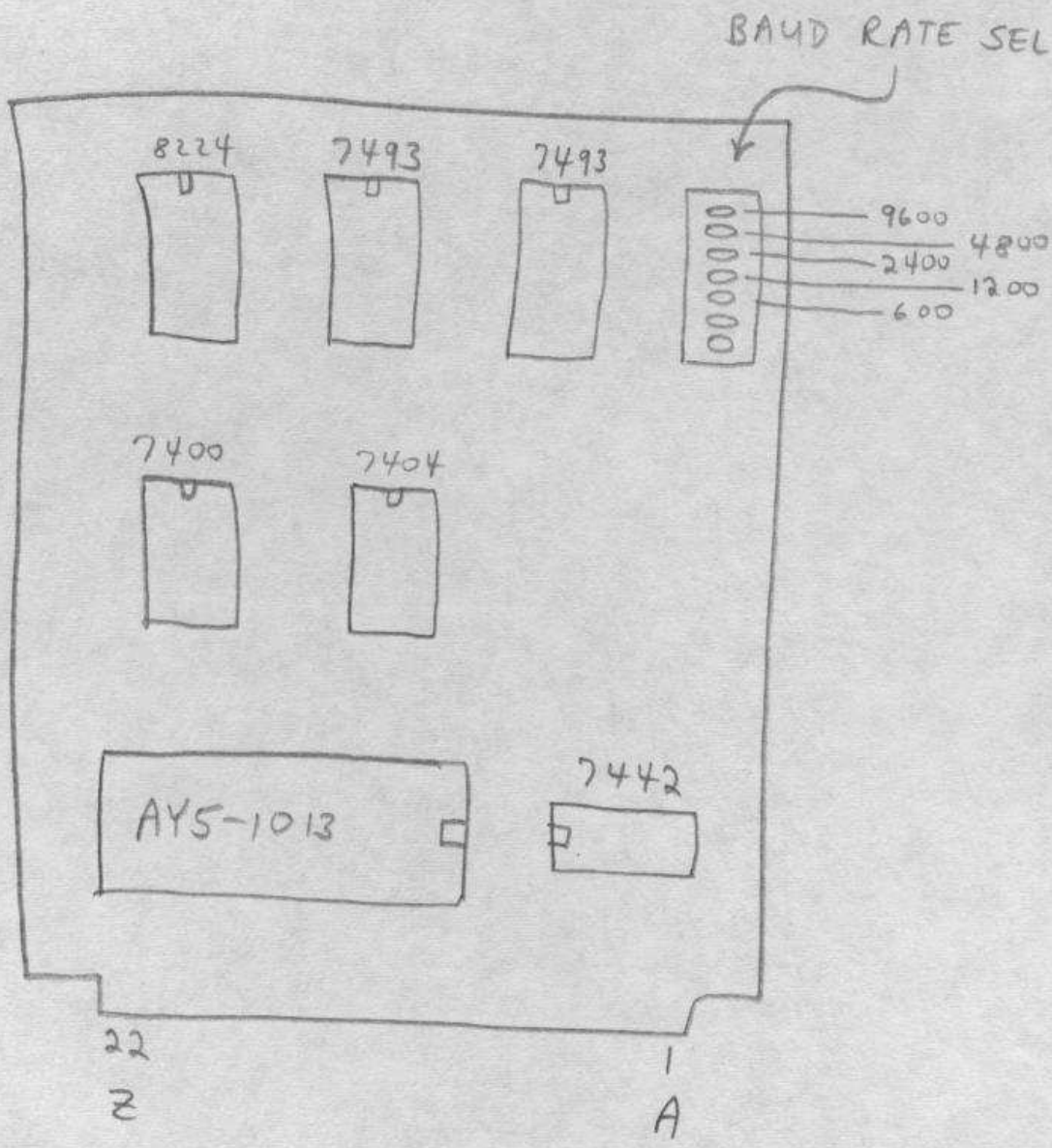
TOP VIEW



A/D CONVERTER CARD

Fig 10

TOP VIEW



SERIAL INTERFACE CARD

Fig 11

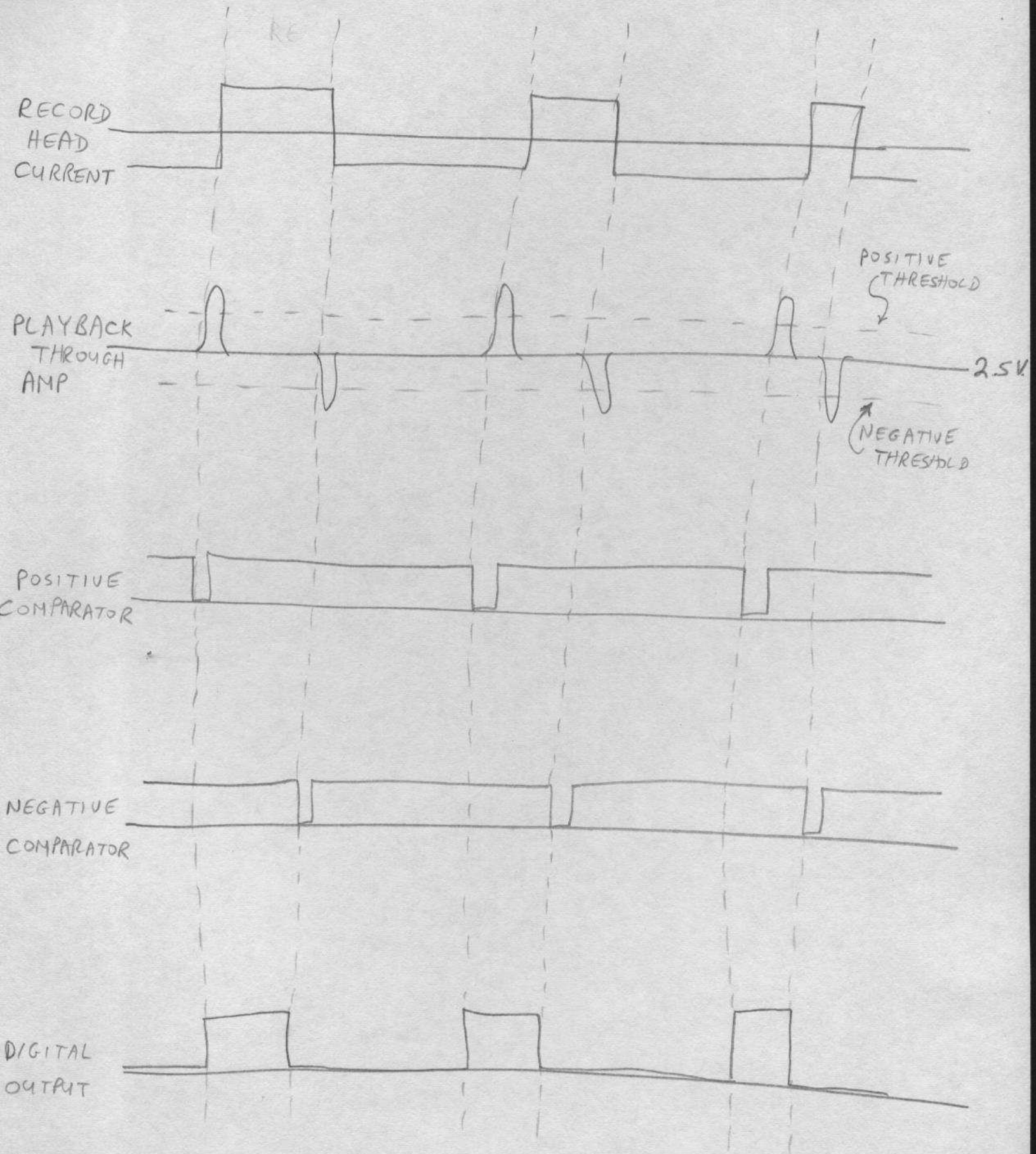


Fig 12 - SIGNAL WAVEFORMS

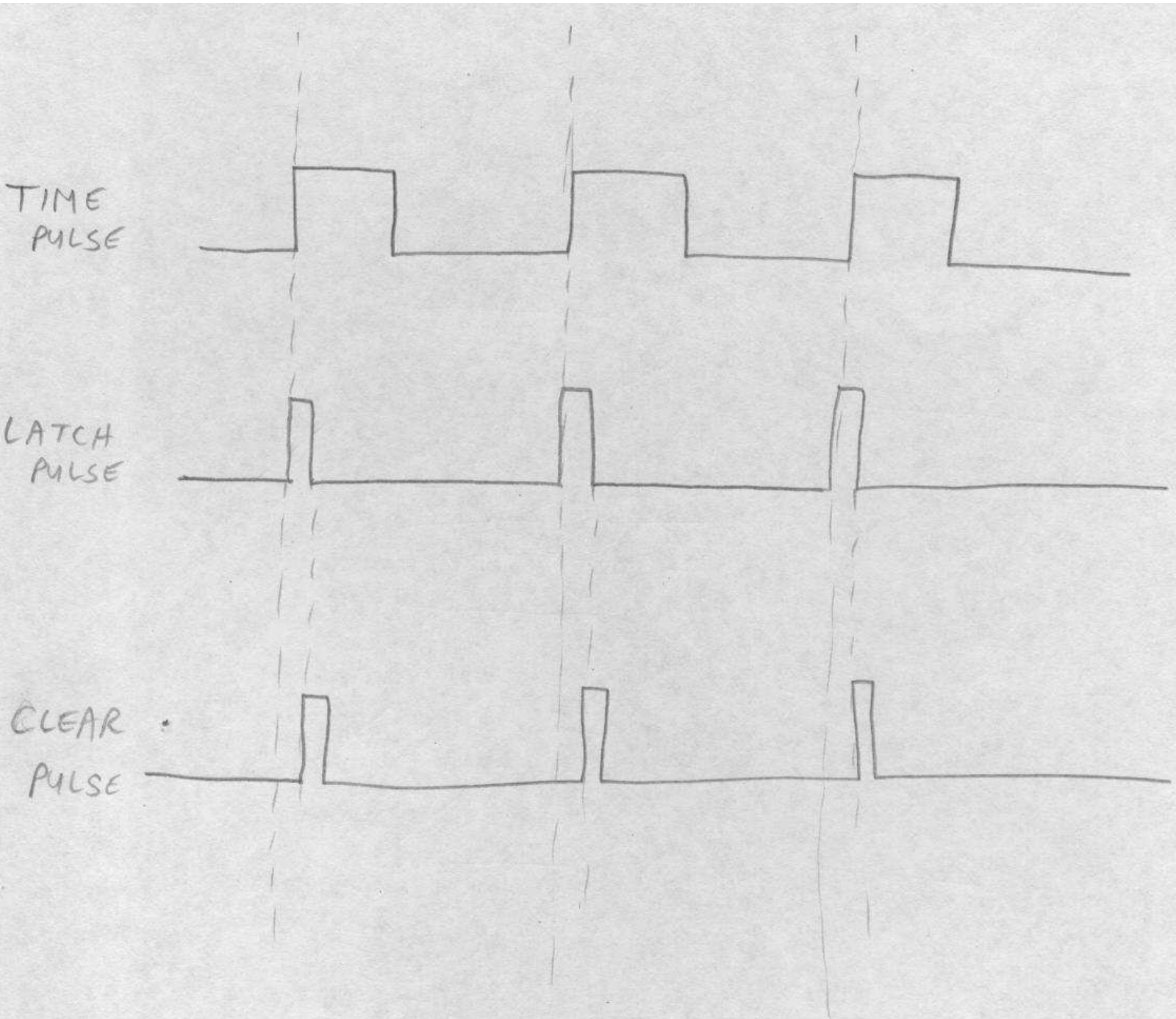
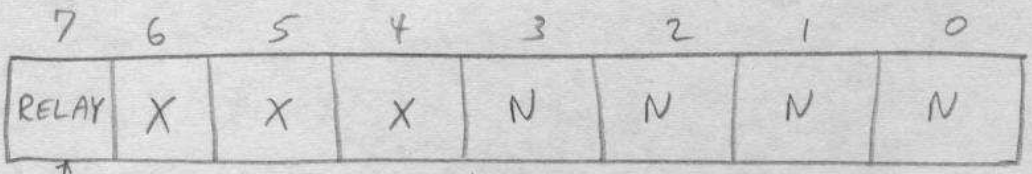


Fig 13 - LATCH AND CLEAR PULSES

Fig 14 - INFORMATION ORGANIZATION

RECEIVED WORD (COMPUTER TO READER) (COMMAND)



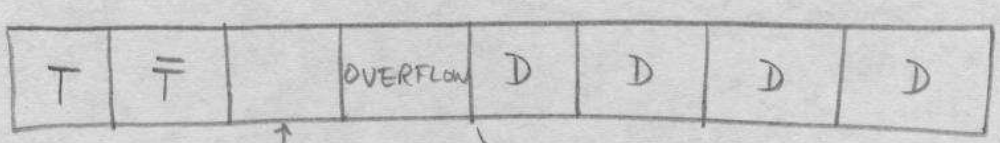
0=OFF
1=ON

X = DON'T CARE

TRANSMIT WORD SELECT
NNNN = 0000 TO 1001
(PORT #)

TRANSMITTED WORDS

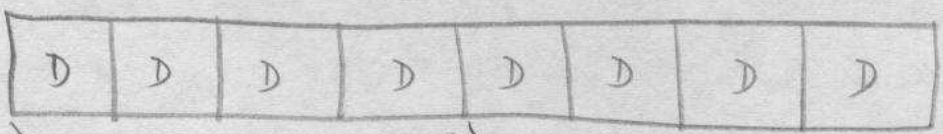
TAPE READER HI (PORT 2, 4, 6)



NEW DATA AVAILABLE
1 = YES
0 = NO
RESET BY READING PORT N-1

BCD, HUNDREDS

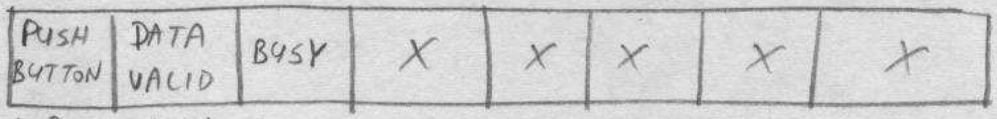
TAPE READER LO (PORT 1, 3, 5)



BCD, TENS

BCD, ONES

CHART READER HI (PORT 8)



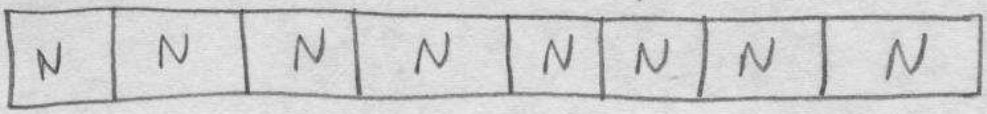
1=PUSHED
0=NOT

1=VALID

1=CONVERTING

X = NOT ASSIGNED

CHART READER LO (PORT 7)



N = 0 TO 255
BINARY POSITION OF POINTER