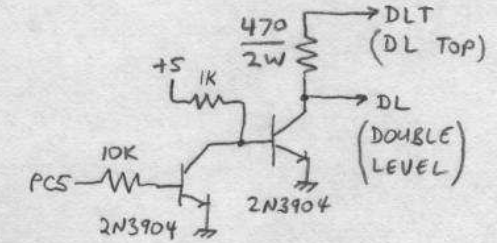
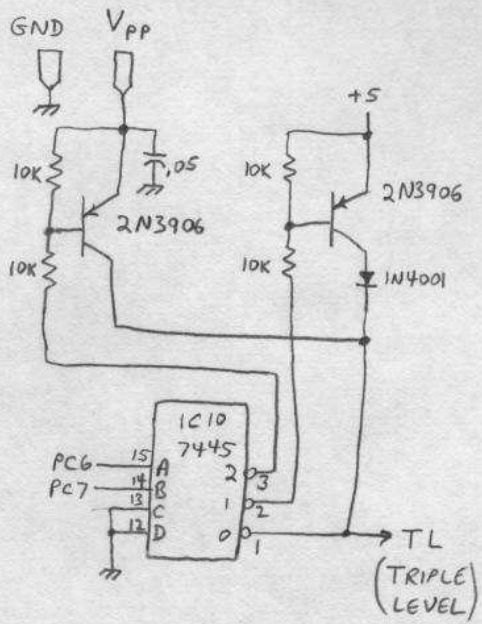


TO EXTERNAL
21-26 V
SUPPLY

TO SYSTEM
BUS



J5:
I/O AB

J6:
I/O C

PA0	1
PA1	2
PA2	3
PA3	4
PA4	5
PA5	6
PA6	7
PA7	8
PB7	9
PB6	10
PB5	11
PB4	12
PB3	13
PB2	14
PB1	15
PB0	16

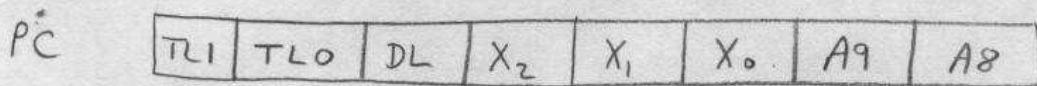
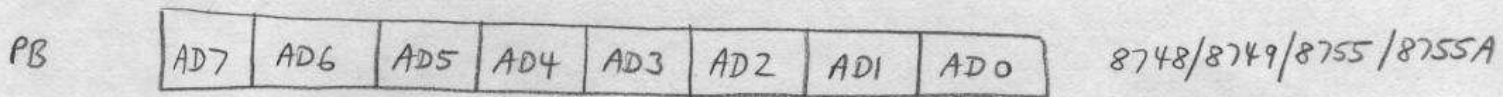
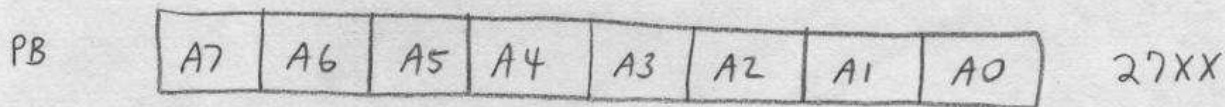
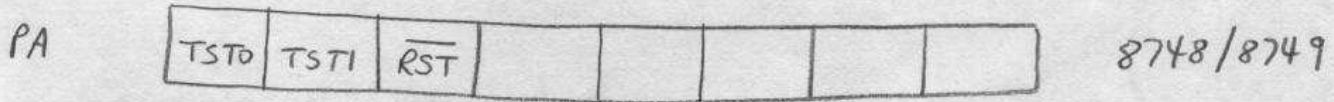
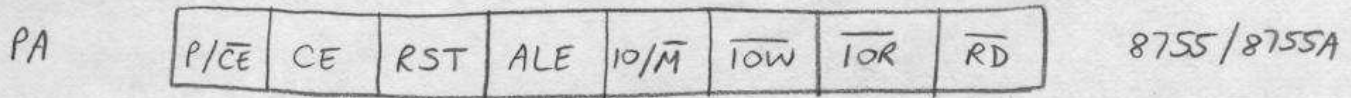
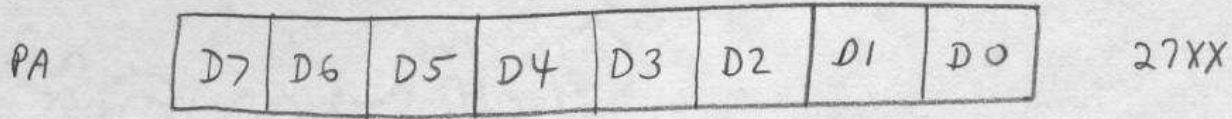
PC0	1
PC1	2
PC2	3
PC3	4
PC4	5
PC5	6
PC6	7
PC7	8
TL	9
DL	10
+12	11
-5	12
Vpp	13
+5	14
	15
	16

IC1, 2, 3, 5, 10:	GND	+5
	8	16
IC4:	7	14
IC9:	7	26



FIG . EPROM PROGRAMMING HARDWARE

7 6 5 4 3 2 1 0



<u>TL1/TL0</u>	<u>TL</u>	<u>TL</u>	<u>DL</u>	<u>DLT</u>
0/0	GND	2704/2708: PGM	2704/2708: \bar{CS}/WE	+12
0/1	+5	2758/2716/2764: V _{PP}	2764: \bar{PGM}	+5
1/0	V _{PP}	2732/2732A: \bar{OE}/V_{PP}	8748/8749: PROG	+25
1/1	HI-Z	8748/8749/8755/8755A: V _{DD}		

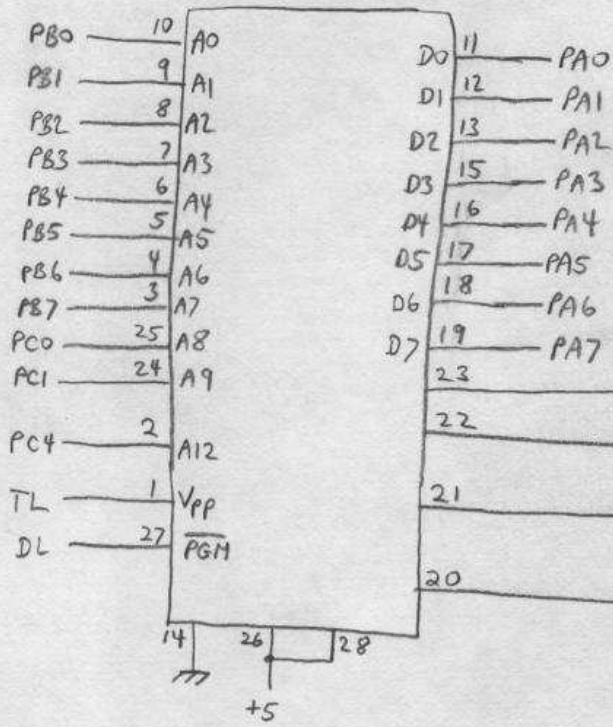
<u>X₀</u>	<u>X₁</u>	<u>X₂</u>	<u>V_{PP}</u>
2758: A ₀	2758/2716: \bar{OE}	2758/2716/	2704/2708: +26V
2716/2732/2732A/	2732/2764: A11	2732/2732A: \bar{CE}	2758/2716/2732/
8755/8755A/8749: A10		2764: A12	8755/8755A/
			8748/8749: +25V
			2732A, 2764: +21V

FIG . PORT ASSIGNMENTS

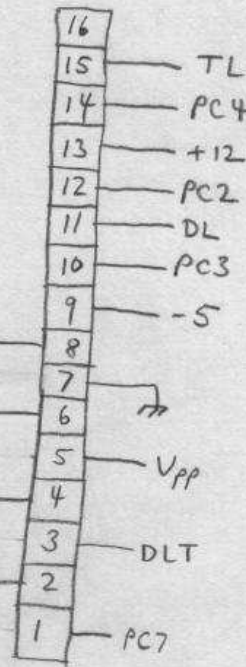
<u>PIN</u>	<u>2704/2708</u>	<u>2758</u>	<u>2716</u>	<u>2732/2732A</u>	<u>2764</u>
18	PGM	\overline{CE}/PGM	\overline{CE}/PGM	\overline{CE}	\overline{CE} (PIN 20)
19	+12	A_R	A_{10}	A_{10}	A_{10} (PIN 21)
20	\overline{CS}/WE	\overline{OE}	\overline{OE}	\overline{OE}/V_{PP}	\overline{OE} (PIN 22)
21	-5	V_{PP}	V_{PP}	A_{11}	A_{11} (PIN 23)
					V_{PP} (PIN 1)
					A_{12} (PIN 2)
					\overline{PGM} (PIN 27)
					+5 (PIN 28)

FIG 1. PINOUT VARIATIONS IN THE INTEL 27XX FAMILY

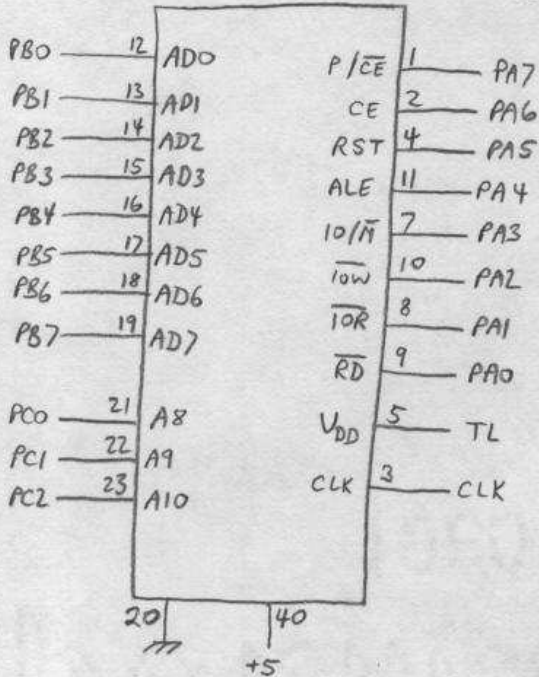
J2 (27XX SOCKET)



J1 (PERSONALITY SOCKET)



J3 (8755/8755A SOCKET)



J4 (8748/8749 SOCKET)

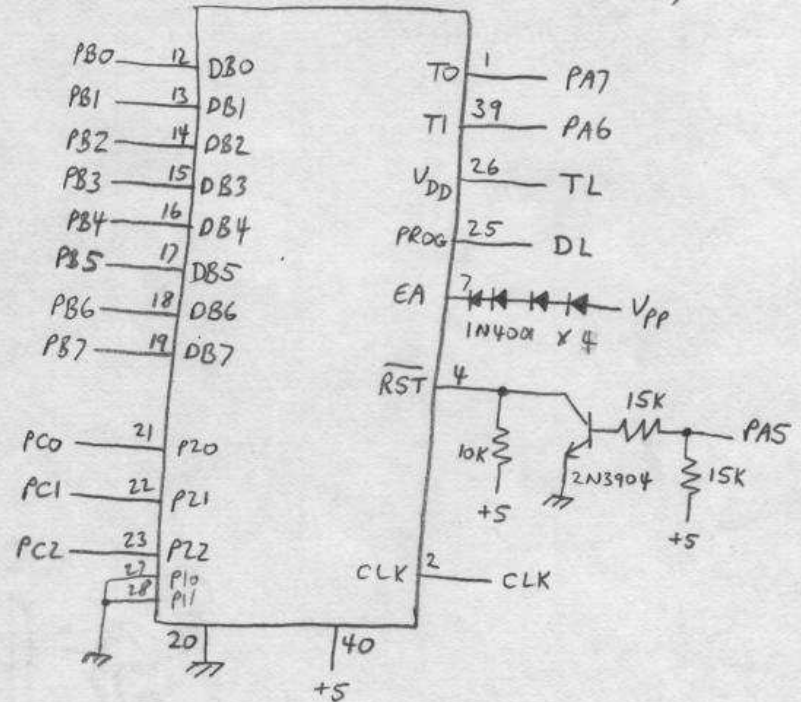
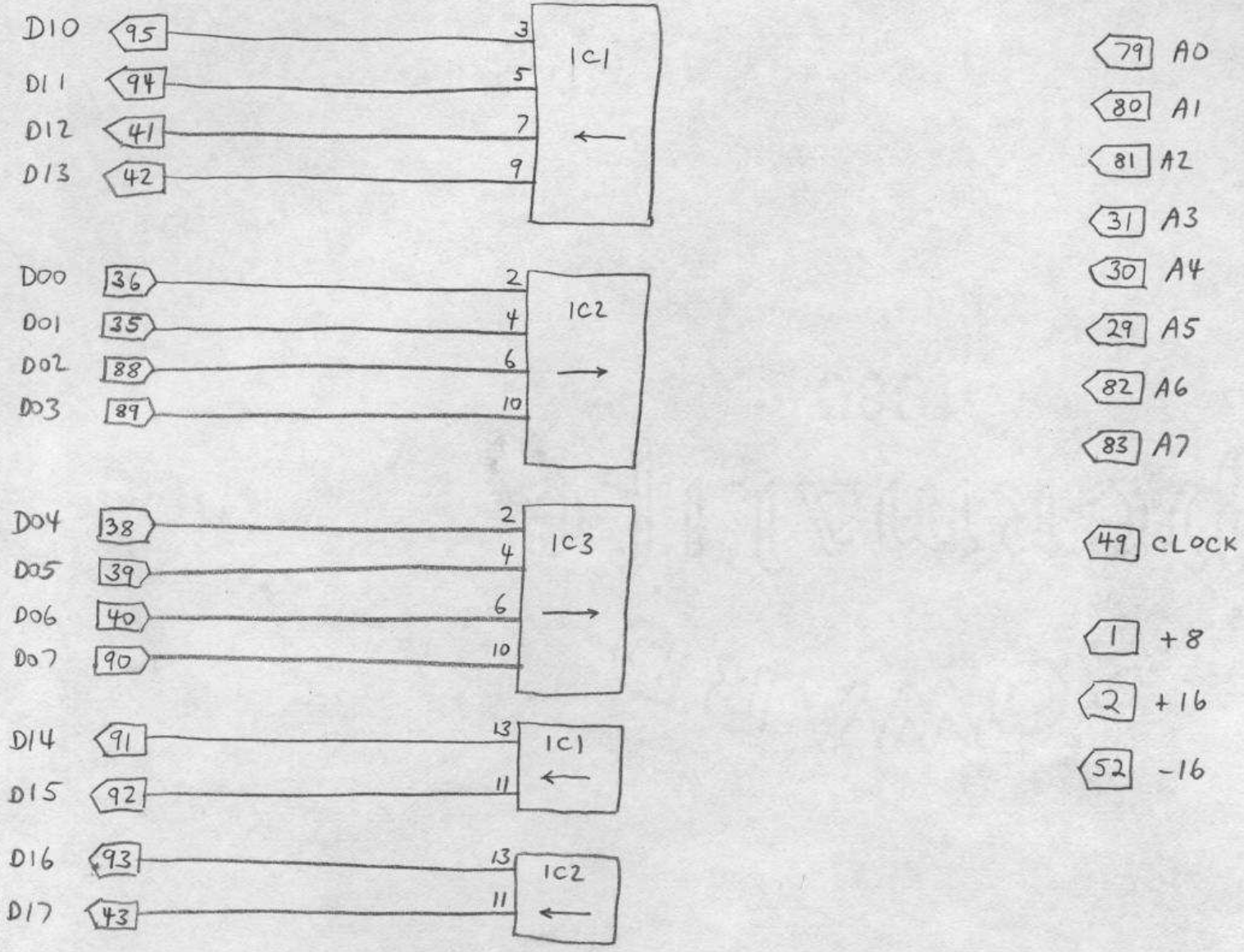


FIG. . EPROM PROGRAMMING HARDWARE, CONTINUED



- 79 A0
- 80 A1
- 81 A2
- 31 A3
- 30 A4
- 29 A5
- 82 A6
- 83 A7
- 49 CLOCK
- 1 +8
- 2 +16
- 52 -16

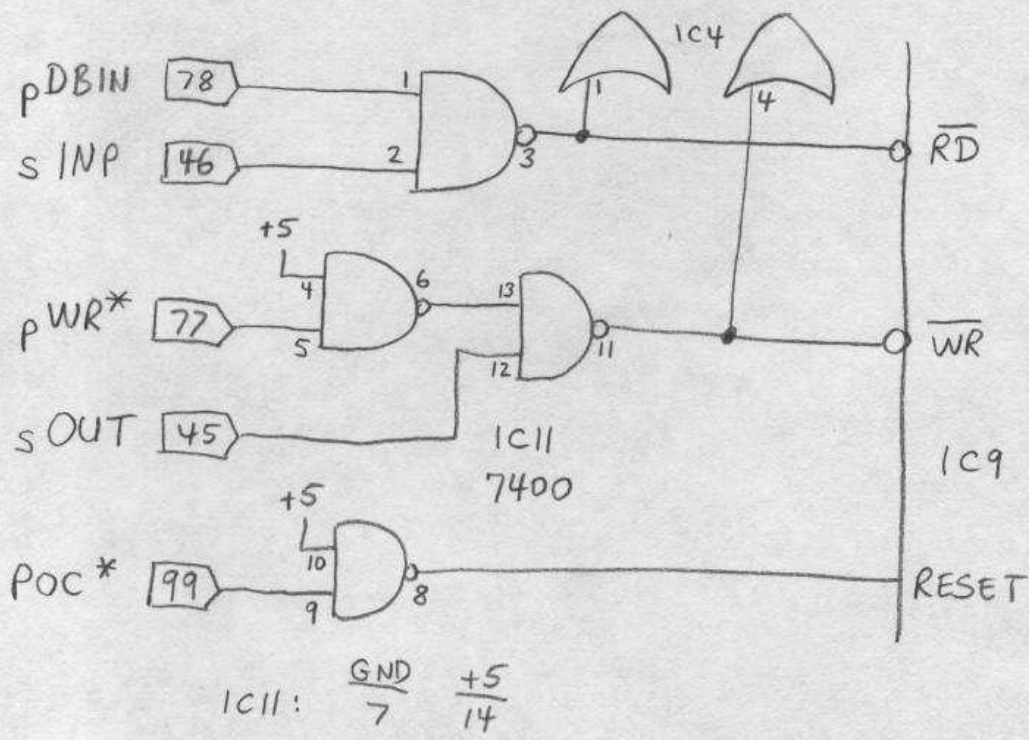
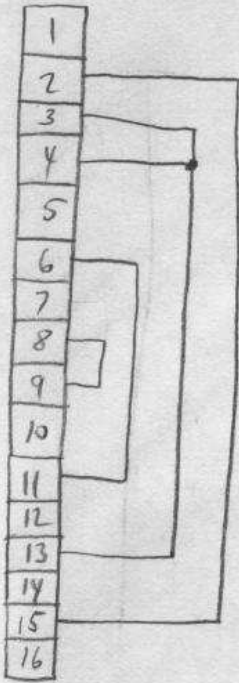
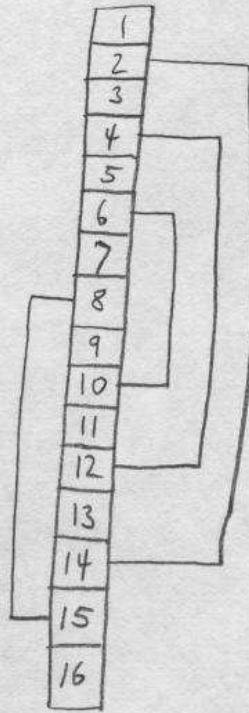


FIG . CONFIGURATION FOR THE S-100 BUS

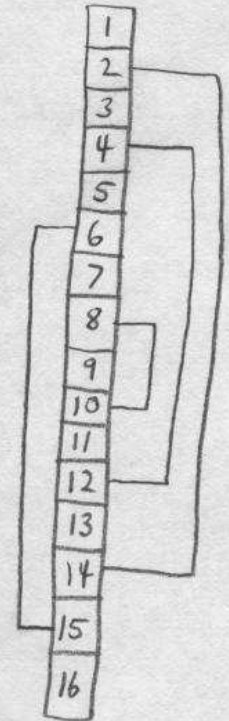
2704/2708



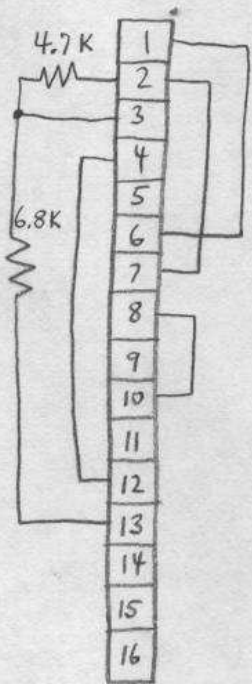
2758/2716



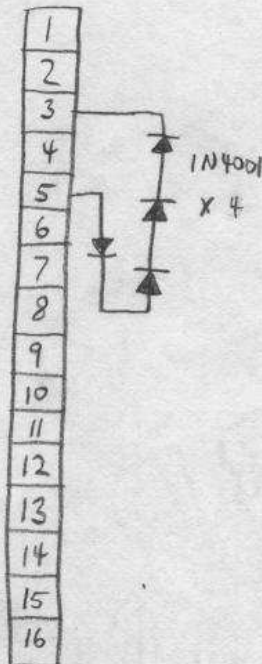
2732/2732A



2764



8748/8749



8755/8755A

NO
CONNECTIONS

FIG . J1 PERSONALITY PLUGS

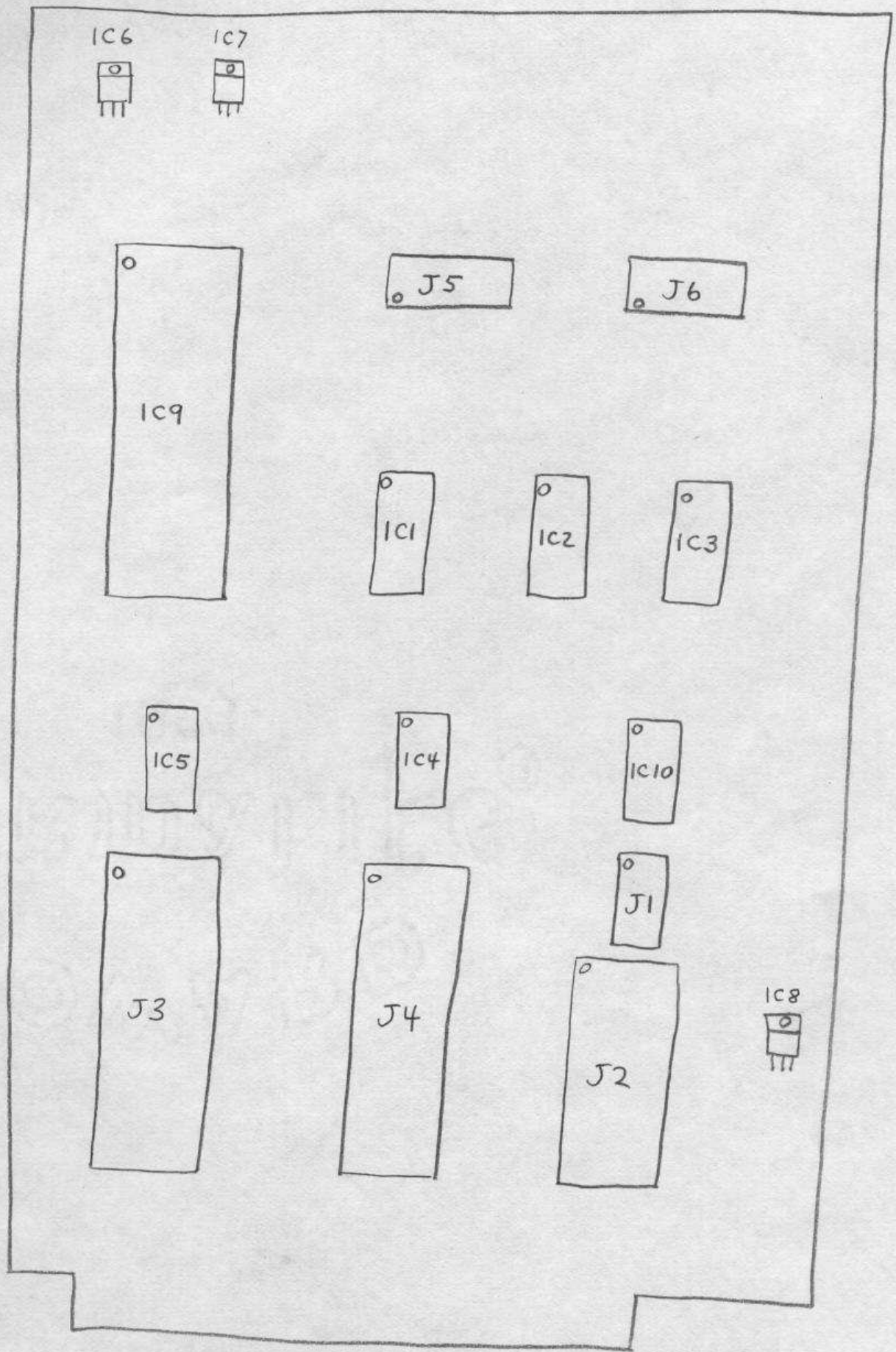


FIG . EPROM PROGRAMMING CARD LAYOUT

